Analog and Digital Electronics

Course Code	L:T:P:S	Credits	Exam marks	Exam Duration	Course Type
18CSI34	3:0:2:0	4	CIE:50 SEE:50	3 Hours	FC

Course Objectives:

This course will enable students to:

- Know the different types of amplifiers constructed from BJTs and MOSFETs.
- Understand applications of diode as clippers, and clampers.
- Apply the theoretical concepts through laboratory and simulation experiments.
- Analyze Synchronous and Asynchronous counters.
- Assess and design sequential circuits.

Syllabus

Module - I

Diode Circuits: The ideal diode, The second approximation, The third approximation, DC resistance of a diode, Load lines, Clippers and Limiters, Clampers.

BJT Amplifiers: Emitter-biased amplifier, Small-signal operation, AC Beta, AC resistance of the emitter diode, Two- transistor models, Analyzing an amplifier, Voltage gain. **08 Hours**

Module - II

MOSFETs: The Depletion-mode MOSFET, D-MOSFET curves, Depletion-mode MOSFET amplifiers, The enhancement-mode MOSFET, CMOS, E-MOSFET amplifiers.

OP-AMP's in Waveform conversion and Generation Circuits: Sine to rectangular, Rectangular to triangular, Triangular to pulse conversion circuits, Relaxation oscillator, Generating triangular waves. **08 Hours**

Module - III

Combinational Logic Circuits: Boolean laws and theorems, Sum-of-Products method, Truth table to Karnaugh map, Pairs Quads, and Octets, Karnaugh simplifications, Don't-care conditions, Product-of-Sums method, Product-of-Sums simplifications, Simplification by Quine-McClusky method, Introduction to HDL, HDL implementation models.

Data-Processing Circuits: Multiplexers, Demultiplexers, 1-of-16 Decoder, Encoders,

08 Hours

Module - IV

Flip-Flops: Introduction, Edge triggered RS FLIP-FLOP, D FLIP-FLOP, JK FLIP-FLOP, T FLIP FLOP, JK Master-slave FLIP-FLOP, Conversion of FLIP FLOPS, Various representation of FLIP-FLOPs,.

08 Hours

Module - V

Registers: Types of Registers, Applications of shift registers.

Counters: Asynchronous counters, Decoding gates, Synchronous counters, changing the counter modulus, Decade counters, Counter design as a synthesis problem.

07 Hours

Course Outcomes:

On completion of this course, the students are able to :

- Use diodes in clippers,and clampers.
- Analyze and design transistor and MOSFET amplifiers in different configura-tions.
- Apply K-Map and Quine-McClusky methods to simplify the given Boolean ex-pressions.
- Design and implement registers using Flip-Flops.
- Design and develop counters using Flip-Flops.

Text Books :

1. Albert Malvino, David Bates: "Electronic Principles", (Chapters 3,4,8,12,20), TMH, New Delhi, 8th Edition, 2015, ISBN-9780073373881.
2. Donald P Leach, Albert Paul Malvino and Goutam Saha: "Digital Principles and Applications", (Chapters 3,4,8- 10), Tata McGraw Hill, New Delhi, India, 8th Edi-tion, 2014, ISBN: 9789339203402.

Reference Books :

1. Robert L. Boylestad, Louis Nashelsky: "Electronic Devices and Circuit Theory", PHI/Pearson Education, New Delhi, 10th Edition, 2012, ISBN: 9788131764596.
2. David A. Bell: "Electronic Devices and Circuits", Oxford University Press, New Delhi, India, 5th Edition, 2010, ISBN: 9780195693409.
3. M Morris Mano: "Digital Logic and Computer Design", Pearson Education, Prentice Hall, 11th Edition, 2009, ISBN: 9788177584097.
4 R D Sudhaker Samuel: "Illustrative Approach to Logic Design", Sanguine-Pearson, New Delhi India, 2012, ISBN: 9788131765081.

E-Resources:

1. https://www.talkingelectronics.com/download/Malvino_electronic_principles. pdf.
2. https://www.rtna.ac.th/departments/elect/data/EE304/Electronic%20Devic-es%20and%20Circuit%20Theory.pdf
3. https://www.abebook.com/Digital_Principles_Applications_Seventh_Edition_ Albert/4893172428/bd

Lab Programs

1. Design and construct a suitable circuit and demonstrate the working of positive clipper, and clamper using diodes.
2. Design and implement relaxation Oscillator using OP-AMP to generate a rectangular wave from for a given frequency.
3. Given a 4-variable logic expression, simplify it using Entered Variable Map and realize the simplified logic expression using 8:1 multiplexer IC.
4. Design and implement a mod-n (n<8) synchronous up counter using J-K Flip-Flop and demonstrate its working.
5. Design and implement a ring counter using 4-bit shift register and demonstrate its working.
6. Demonstrate the working of the positive clipper and clamper circuits.
7. Build relaxation Oscillator using a simulation package and verify its waveforms.
8. Develop the Verilog / VHDL code for an 8:1 multiplexer. Simulate and verify its working.
9. Develop the Verilog / VHDL code for D Flip-Flop with positive-edge triggering. Simulate and verify its working.

10.Develop the Verilog / VHDL code for switched tail counter. Simulate and ver-ify its working.